WHAT IS CLAIMED IS:

1. A parallel processor that performs parallel processing of one or more basic instructions contained in each of instruction words delimited by instruction delimiting information, said parallel processor comprising:

a plurality of instruction execution units that perform processes corresponding to supplied basic instructions in parallel;

an instruction fetch unit that fetches the instruction words one by one in accordance with the instruction delimiting information; and

an instruction issue unit that selectively issues each of the basic instructions supplied from the instruction fetch unit to one of the instruction execution units to execute an issued basic instruction.

2. The parallel processor as claimed in claim 1, wherein the plurality of instruction execution units all have the same structure.

3. The parallel processor as claimed in claim 1, wherein:

at least two of the instruction execution units have different structures from each other; and

the instruction fetch unit rearranges the

basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the plurality of instruction execution units, and then supplies the rearranged basic instructions to the instruction issue unit.

4. The parallel processor as claimed in claim 1, wherein:

at least two of the instruction execution units have different structures from each other; and

the instruction issue unit rearranges the basic instructions contained in each of the instruction words supplied from the instruction fetch unit, in accordance with arrangement of the plurality of instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units.

5. The parallel processor as claimed in claim 1, wherein:

at least two of the instruction execution units have different structures from each other;

the instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction issue unit; and

the instruction issue unit further rearranges the basic instructions contained in each of the instruction word supplied from the

instruction fetch unit, in accordance with the arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units.

6. The parallel processor as claimed in claim 3, wherein:

at least two of the instruction execution units have different structures from each other; and

the instruction fetch unit fetches an instruction word that contains basic instruction arranged in advance in accordance with the arrangement of the instruction execution units.

7. The parallel processor as claimed in claim 1, wherein, depending on the type of a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues a next basic instruction before the execution of a basic instruction being currently executed is completed.

8. The parallel processor as claimed in claim 7, wherein, if a supplied basic instruction does not have data dependency or control dependency, or does not share resources with a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues

the supplied basic instruction before the execution of the basic instruction being currently executed is completed.

B1

5